IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (canceled)

Claim 2 (currently amended): A semiconductor memory ~~according to claim 1~~ comprising:

a first and a second field effect transistors having a first line as gates, one ends of current paths of the first and second field effect transistors being connected to a reference electrode supplied with a reference potential;

a third and a fourth field effect transistors having a second line as gates, one ends of current paths of the third and fourth field effect transistors being connected to the reference electrode;

a fifth field effect transistor having a first word line as a gate, one end of a current path of the fifth field effect transistor being connected to the other ends of the current paths of the first and second field effect transistors; and

a sixth field effect transistor having a second word line as a gate, one end of a current path of the sixth field effect transistor being connected to the other ends of the current paths of the third and fourth field effect transistors,

wherein the current paths of the first and second field effect transistors are connected in parallel between the one end of the current path of the fifth field effect transistor and the reference electrode, and

the current paths of the third and fourth field effect transistors are connected in parallel between the one end of the current path of the sixth field effect transistor and the reference electrode.

Claim 3 (currently amended): A semiconductor memory according to claim [[1]] 2, wherein each of the first, second, third, fourth, fifth and sixth transistors includes a fin typed field effect transistor.

Claim 4 (currently amended): A semiconductor memory according to claim [[1]] 2, wherein each of the first, second, third and fourth transistors forms a drive transistor, and each of the fifth and sixth transistors forms a transfer gate transistor.

Claim 5 (currently amended): A semiconductor memory according to claim [[1]] 2, further comprising: a seventh field effect transistor having the first line as a gate; and an eighth field effect transistor having the second line as a gate.

Claim 6 (original): A semiconductor memory according to claim 5, wherein one ends of current paths of the seventh and eighth field effect transistors are connected to a power supply electrode supplied with a power supply voltage.

Claim 7 (original): A semiconductor memory according to claim 5, wherein the other ends of the current paths of the first and second field effect transistors are connected to the other end of the current path of the seventh field effect transistor, and

the other ends of the current paths of the third and fourth field effect transistors are connected to the other end of the current path of the eighth field effect transistor.

Claim 8 (original): A semiconductor memory according to claim 5, wherein the gates of the first, second and seventh field effect transistors are connected to the other ends of the current paths of the third and fourth field effect transistors, and the gates of the third, fourth and eighth field effect transistors are connected to the other end of the current path of the seventh field effect transistor.

Claim 9 (original): A semiconductor memory according to claim 5, wherein the first, second, fifth and seventh field effect transistors are symmetrical to the third, fourth, sixth and eighth field effect transistors, respectively, with respect to a certain point.

Claim 10 (canceled)

Claim 11 (currently amended): A semiconductor memory ~~according to claim 10, wherein~~ comprising:

a first and a second field effect transistors having a first line as gates, one ends of current paths of the first and second field effect transistors being connected to a first reference electrode supplied with a reference potential;

a third and a fourth field effect transistors having a second line as gates, one ends of current paths of the third and fourth field effect transistors being connected to a second reference electrode supplied with the reference electrode;

a fifth field effect transistor having a first word line as a gate, one end of a current path of the fifth field effect transistor being connected to the other ends of the current paths of the first and second field effect transistors; and

a sixth field effect transistor having a second word line as a gate, one end of a current path of the sixth field effect transistor being connected to the other ends of the current paths of the third and fourth field effect transistors,

wherein the first, second and fifth field effect transistors are arranged symmetrically to the third, fourth and sixth field effect transistors, respectively, with respect to a central point between the fifth field effect transistor and the sixth field effect transistor,

the current paths of the first and second field effect transistors are connected in parallel between the one end of the current path of the fifth field effect transistor and the first reference electrode, and

the current paths of the third and fourth field effect transistors are connected in parallel between the one end of the current path of the sixth field effect transistor and the second reference electrode.

Claim 12 (currently amended): A semiconductor memory according to claim [[10]] 11, wherein each of the first, second, third, fourth, fifth and sixth transistors includes a fin typed field effect transistor.

Claim 13 (currently amended): A semiconductor memory according to claim [[10]] 11, wherein each of the first, second, third and fourth transistors forms a drive transistor, and each of the fifth and sixth transistors forms a transfer gate transistor.

Claim 14 (currently amended): A semiconductor memory according to claim [[10]] 11, further comprising: a seventh field effect transistor having the first line as a gate; and an eighth field effect transistor having the second line as a gate.

Claim 15 (original): A semiconductor memory according to claim 14, wherein one ends of current paths of the seventh and eighth field effect transistors are connected to a power supply electrode supplied with a power supply voltage.

Claim 16 (original): A semiconductor memory according to claim 14, wherein the other ends of the current paths of the first and second field effect transistors are connected to the other end of the current path of the seventh field effect transistor, and

the other ends of the current paths of the third and fourth field effect transistors are connected to the other end of the current path of the eighth field effect transistor.

Claim 17 (original): A semiconductor memory according to claim 14, wherein the gates of the first, second and seventh field effect transistors are connected to the other ends of the current paths of the third and fourth field effect transistors, and

the gates of the third, fourth and eighth field effect transistors are connected to the other end of the current path of the seventh field effect transistor.

Claim 18 (currently amended): A semiconductor memory comprising:

a group of drive transistors including a plurality of field effect transistors, each of which having a current path having one end connected to a reference electrode supplied with a reference potential; and

a group of transfer gate transistors including a plurality of field effect transistors, each of which having a word line as a gate and having a current path with one end connected to the other ends of the current paths ~~of two~~ of the field effect transistors included in the drive transistor group, the number of the field effect transistors of the transfer gate transistor group being smaller than the number of the field effect transistors included in the drive transistor group,

wherein the current paths of the field effect transistors included in the drive transistor group are connected in parallel between the one end of the current path of one of the field effect transistors included in the transfer gate transistor group and the reference electrode.